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PATENT
Attorney Dkt: 2540-6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 5,732,212

Issue Date: March 24, 1998

In re Reissue Application of:

Perholtz, Ronald J. et al.

Serial No.: 08/180,824

Filed: January 13, 1994

Group Art Unit: 2308

Examiner: Mehmet Geckil

For: SYSTEM AND METHOD FOR REMOTE MONITORING AND OPERATION OF PERSONAL COMPUTERS

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner for Patents
BOX PATENT APPLICATION
Washington, DC 20231

Sir:

As suggested by 37 C.F.R. 1.97, the undersigned attorney brings to the attention of the Patent and Trademark Office the references listed on the attached form PTO-1449, a copy of each of which is enclosed.

Citation of a reference herein is not necessarily to be construed that the reference constitutes prior art with respect to the captioned application. In fact, some references

cited herein are for the benefit of the Examiner in connection with a simultaneously filed Request For Interference.

Selected references are discussed below for convenience of the Examiner.

(1) Motorola Semiconductor Technical Data Sheet Product Preview Advanced Monitor On-Screen Display, Document Order No. MC141543/D, Rev. 0, January 1995.

This reference describes the On Screen Display 364 (shown in Fig. 12A) of US Patent 5,721,842 to Beasley. Applicants seek to provoke an interference with respect to claims 1 and 2 of the US Patent 5,721,842 to Beasley, and to have at least claims 1 - 3 and 8 - 17 of US Patent 5,721,842 to Beasley declared as corresponding to Proposed Count 1.

(2) Service Manual, Multi-Scan Color CRT Display Model No. MDSP12909 (TX-D1751W) September 1994

This reference illustrates how the On Screen Display of reference (1) above, e.g., chip MC141543/D, can be incorporated into a system which also utilizes the following:

- a signal generator for generating internal horizontal and vertical synchronize signals (see, e.g., H/V PROCESS CIRCUIT [IC501] shown, e.g., on Block Diagram p. 39).

- a synchronize switch (see, e.g., H/V PROCESS CIRCUIT [IC501] (see, e.g., Block Diagram p. 39) which receives internal horizontal and vertical synchronize signals produced by the signal generator and the external horizontal and vertical synchronize signals received from the external source, and selects either the internal or external synchronize signals to be applied to an on-screen programming circuit [see, e.g., ON SCREEN DISPLAY PATTERN

on-screen programming circuit [see, e.g., ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] in Block Diagram p. 36 of reference (2)].

- a first set of buffer circuits having inputs coupled to receive the video signals produced by the external source and a second set of buffer circuits having inputs coupled to receive the video signals produced by an on-screen programming circuit [see, e.g., the VIDEO BUFFER (see, e.g., Block Diagram p. 37 of reference (2)].

- control logic circuit that enables the first and second set of buffer circuits so that video signals supplied are either the video signals produced by the external source, or the video signals produced by an on-screen programming circuit or both [see, e.g., the signal FBKG and ANALOG SWITCH [IC1308] in Block Diagram p. 37 of reference (2)].

- a synchronize polarizer circuit which receives the internal or external horizontal or vertical synchronize signals selected by the synchronize switch and which converts the selected US horizontal and vertical synchronize signals to active-low logic levels [see, e.g., IC201 of SYNC SEPARATOR MODE DETECTOR and INVERTER IC203 shown, e.g., in Block Diagram p. 36 of reference (2)].

- a decoder circuit for removing the horizontal and vertical sync signals from a red, green, or blue video signal [see, e.g., SYNC ON GREEN capability provided by SYNC SEPARATOR MODE DETECTOR [IC201, Q250 Q251] in Block Diagram p. 36 of reference (2)].

Reference (2) is selectively summarized below:

The CRT display can be connected by either of two types of connectors to receive input from an external source: (1) a BNC connector or (2) a 15 pin D_SUB connector (see, e.g., Block Diagram p. 36). Either type of connector supplies external red (R), green (G), and blue (B) signals, along with an external horizontal sync/vertical sync mix signal (HS/HV MIX). A VIDEO SELECT circuit selects from which connector to obtain the external red (R), green (G), and blue (B) signals (see, e.g., Block Diagram p. 36). A SYNC SELECT circuit (see, e.g., Block Diagram p. 36) selects from which connector to obtain the external HS/HV MIX signal. Once selected, the external horizontal sync signal (HS) and external vertical sync signal (VS) from the external source are separated by a SYNC SEPARATOR MODE DETECTOR [IC201, Q250 Q251] (see, e.g., Block Diagram p. 36). With respect to the BNC connector external input, a SYNC ON GREEN capability is provided with SYNC SEPARATOR MODE DETECTOR [IC201, Q250 Q251] (see, e.g., Block Diagram p. 36) serving to decode the sync signal from the green signal.

The external horizontal sync signal (HS) and external vertical sync signal (VS) are applied to a H/V PROCESS CIRCUIT [IC501] (see, e.g., Block Diagram p. 39). The H/V PROCESS CIRCUIT [IC501] is a synchronize switch since it selects between the external sync signals (i.e., external horizontal sync signal (HS) and external vertical sync signal (VS)) and internally generated sync signals for application of resultant sync signals to an ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] (see, e.g., Block Diagram p. 36). In particular, the resultant sync signals applied to an ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] are signals V_PULSE and H_PULSE (see, e.g., Block Diagram p. 36). The resultant vertical sync signal V_PULSE is derived from signal VD outputted from H/V PROCESS CIRCUIT [IC501]; the resultant horizontal sync signal H_PULSE is derived from signal HD outputted from H/V PROCESS CIRCUIT [IC501] (see output H_DRIVE).

H/V PROCESS CIRCUIT [IC501] (see, e.g., Block Diagram p. 39) generates the internal sync signals. The H/V PROCESS CIRCUIT [IC501] has a free running oscillator which generates an internal vertical synchronize signal and a horizontal synchronize signal. When the external synchronize signals are not to be outputted by H/V PROCESS CIRCUIT [IC501] , H/V PROCESS CIRCUIT [IC501] outputs the internal sync signal on line VD (pin 24) and the internal horizontal synchronize signal on line H_DRIVE (pin 16).

The synchronize signals selected by H/V PROCESS CIRCUIT [IC501] are ultimately applied as horizontal synchronize signal (H_PULSE) and vertical synchronize signal (V_PULSE) to ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] (see, e.g., Block Diagram p. 36). The horizontal synchronize signal (H_PULSE) and vertical synchronize signal (V_PULSE) are always the same polarity (active low) regardless of input polarity, as ensured by the SYNC SEPARATOR MODE DETECTOR (see, e.g., Block Diagram, p. 36). In the schematics, IC201 is shown on page 52. The horizontal synchronize signal HS out of pin 15 of IC201 is HD. Signal HD is routed (via pages 53 and 54) to IC501 on page 55. For the horizontal synchronize , IC201 accomplishes polarity correction since pin 15 out of IC501 is always a negative sync signal, regardless of the horizontal synchronize input to IC501 (at pin 6). For the vertical synchronize signal, the vertical synchronize signal input VIN on pin 8 of IC201 is output at pin 13. The polarity of the vertical synchronize signal is corrected at IC203 (page 52). In this regard, the vertical synchronize signal on line VD output by IC201 is applied to pins 9 and 10 of IC203, where it is corrected and output as low signal VS on pin 8. For vertical synchronize signals, IC201 and IC203 serve as a synchronize polarizer circuit.

The ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] generates overlaying video signals OSD_R, OSD_G, OSD_B (see, e.g., Block Diagram p. 36). Both the external source video signals [(R), (G), and (B)] and the video signals generated

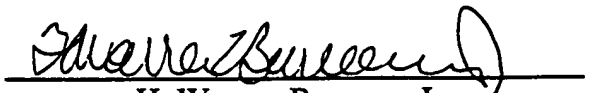
by the ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] (OSD_R, OSD_G, OSD_B) are applied to a VIDEO BUFFER (see, e.g., Block Diagram p. 37). The VIDEO BUFFER comprises a first set of buffer circuits having inputs coupled to receive the video signals produced by the external source [(R), (G), and (B)] and a second set of buffer circuits having inputs coupled to receive the video signals produced by ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] (OSD_R, OSD_G, OSD_B). The first and second sets of buffers are shown in more detail as drivers on page 53 of reference (2), particularly in the upper center portion of the page.

A signal FBKG applied to ANALOG SWITCH [IC1308] (see, e.g., Block Diagram p. 37) is employed to select between the first set of buffers and the second set of buffers, the signal FBKG being output by SCREEN DISPLAY PATTERN GENERATOR [IC1305] (see, e.g., Block Diagram p. 36). The signal FBKG and ANALOG SWITCH [IC1308] thus comprise a control logic circuit that enables the first and second set of buffer circuits so that video signals supplied are either the video signals produced by the external source, or the video signals produced by the ON SCREEN DISPLAY PATTERN GENERATOR [IC1305] or both.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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Sheet 1 of 1

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY. DOCKET NO.	PATENT NO./REISSUE APP
2540-6	5,732,212/UNKNOWN
APPLICANT	
Perholtz et al.	
REISSUE FILING DATE	GROUP
SIMULTANEOUS	2308

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		G 9203884.0	3/24/92	Germany			partial	
		G 9010535.4	7/11/90	Germany			partial	
		GB 2249645A	7/11/90	United Kingdom				

OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

		Service Manual, Multi-Scan Color CRT Display Model No. MDSP12909 (TX-D1751W) September 1994
		Advanced Monitor On-Screen Display, Document Order No. MC141543/D, Rev. 0, January 1995.
		Reachout Remote Control for Windows and DOS, User Guide Version 2.1, Ocean Isle Software, July 2, 1992

*Examiner		Date Considered	

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449)